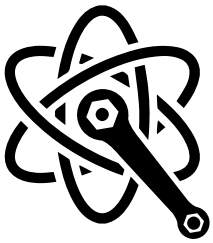

ARTIQ
Status report

October 3rd, 2017

1 General ARTIQ software

1.1 New releases

After a year since the last major release, we are pleased to announce ARTIQ 3.0.

There were about 1300 commits since 2.0, for many different features such as RTIO DMA that can dramatically improve the throughput of long pulse sequences, and asynchronous RPCs to speed up the reporting results from the core device, and dashboard applet control from experiments.

ARTIQ-3 contains demonstrations on the KC705 board for two new major features that will be fully developed in ARTIQ-4 on the Sinara hardware: distributed RTIO and the SAWG. We also made major improvements to the PDQ waveform generator, which take advantage of ARTIQ-3 features.

The core device runtime saw a complete rewrite in Rust, and it now uses a new TCP/IP stack that we developed that should fix stability and performance issues encountered with lwIP.

During the last month, we have fixed the last remaining bugs in that TCP/IP stack, which were delaying the release of 3.0.

We also released a minor bugfix 2.5 release to the ARTIQ-2 series, for users who do not wish to upgrade to ARTIQ-3 at this time.

1.2 Scalable Event Dispatcher (fka. SRTIO)

We have implemented a new RTIO architecture, discussed in GitHub issue 778 and described in `artiq/gateware/rtio/sed/__init__.py` on the `rtio-sed` branch. This architecture allows more RTIO channels to be efficiently implemented in a single device, and makes DRTIO switching easier to develop and reduces its resource demands on the master.

We have developed, integrated and tested it in functional simulation and on the hardware, for local and DRTIO remote channels. All the unit tests are passing except the DMA ones. There is an unexpected performance bug with DMA that needs investigating and fixing (GitHub issue 834).

2 Sinara hardware

2.1 Sayma and Allaki

We have found and fixed the problems that were preventing the JESD204B links from working on the Sayma prototypes, and have now validated DAC operation.

Following this milestone, the production of Allaki and 8 Sayma RTM boards is under way.

2.2 Kasli and Urukul

Layout is nearing completion and power supply integrity and signal integrity analyses are being performed.

2.3 Novogorny

The characterization of the 8 channel ADC Novogorny is near completion and confirms the excellent low noise, high CMRR, and low crosstalk specifications.

2.4 RF PA

The RF PA prototypes have been built and are being tested.

2.5 Clocker

Clocker (`https://github.com/m-labs/sinara/wiki/Grabber`) is a new EEM for low noise clock distribution. Its PCB design has been finished.

3 Sinara software support

3.1 OpenOCD and proxy bitstreams

The JTAGSPI protocol has been rewritten to work in more corner cases of multiple TAPs and be more robust toward idiosyncratic SPI flash memories. It was debugged on Sayma, KC705, and multiple non-Sinara customer boards.

3.2 Clock chip programming

We have written the ARTIQ firmware code to automatically program the HMC830 and HMC7043 chips on the Sayma RTM cards. Tests on the hardware have been delayed due to the restricted availability of RTM cards.

See the files: `artiq/firmware/libboard/hmc*`

3.3 JESD204B/SAWG

The JESD204B links between the Sayma AMC FPGA and the AD9154 DACs have been debugged and verified up to 10 GBit/s. Integration of the Smart Arbitrary Waveform Generator (SAWG) into the Sayma bitstream is under way.

See for example the Sayma AMC target file:
`artiq/gateware/targets/sayma_amc_standalone.py`