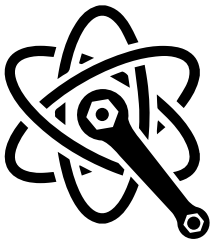

ARTIQ
Status report

April 7th, 2018

1 DRTIO

1.1 Stack

We have implemented the fix for the Si5324 phase determinism and wander issues. The full stack on Kasli demonstrated timing stability between a master and a satellite better than 100ps, including across reboots. The DRTIO system has been comprehensively tested, and is now fully functional on Kasli.

Sayma does not show any obvious problems, but has received less testing than Kasli.

1.2 Fine RTIO clock

We have implemented a clock multiplier to generate a fine RTIO clock that is aligned to the DRTIO recovered clock. This allows the use of high-resolution SERDES TTLs in DRTIO systems.

On Kasli, with a 7-series FPGA, this was done without particular difficulties using a MMCM.

On Sayma, due to flaws in the Ultrascale architecture, this simple clocking topology does not meet timing constraints (TPWS) at the IOSERDES. During discussions with Xilinx technical support, we arrived at a solution that involves generating both the coarse and fine RTIO clocks from the GTH transceiver system. It remains to be implemented and tested.

2 Sinara hardware

2.1 Organization

The Sinara hardware repositories have been moved to `https://github.com/sinara-hw`.

There is now one repository per project (Kasli, Urukul etc.), and they have been cleaned up (no temporary files etc.)

The splitting and cleaning up is still underway for some projects such as Sayma.

2.2 Sampler

The 8 channel SPI ADC has received comprehensive testing and the ARTIQ core device driver was added to the tree. Production of the first larger batch is underway.

2.3 Zotino

The 32 channel SPI DAC has been tested and the ARTIQ core device driver has been updated. Production of the first larger batch is underway.

2.4 Sayma

2.4.1 DDR3 SDRAM

The Kintex Ultrascale DDR3 PHY interface as well as the MiSoC/ARTIQ SDRAM leveling algorithms have been reviewed and improved. The data from the available Sayma boards indicates that the SDRAM interface is now working reliably.

2.4.2 High-resolution TTLs

We have implemented high-resolution TTLs on Ultrascale based on the IOSERDES. We have not tested them yet due to difficulties finding a clocking solution that would work on both standalone and DRTIO systems.

2.4.3 DRTIO

We have debugged and finalized support for multiple links on DRTIO masters on Sayma.

2.5 Kasli

We have fixed the timing closure issues with ARTIQ bitstreams on Kasli, by reducing the CPU clock frequency by a few percent. We are considering using a faster FPGA speed grade on the next board revision.

Conda packages for Kasli targets are now built by the buildbot.

3 PTB drivers

More drivers for PTB hardware, including a multichannel temperature measurement device, have been developped as out-of-tree drivers for ARTIQ. `https://github.com/quartiq/ptb-drivers`

4 ARTIQ 3.6

We have released new bugfix versions of ARTIQ, which mostly address core device crashes and Windows-specific problems. We recommend that all users update to 3.6.