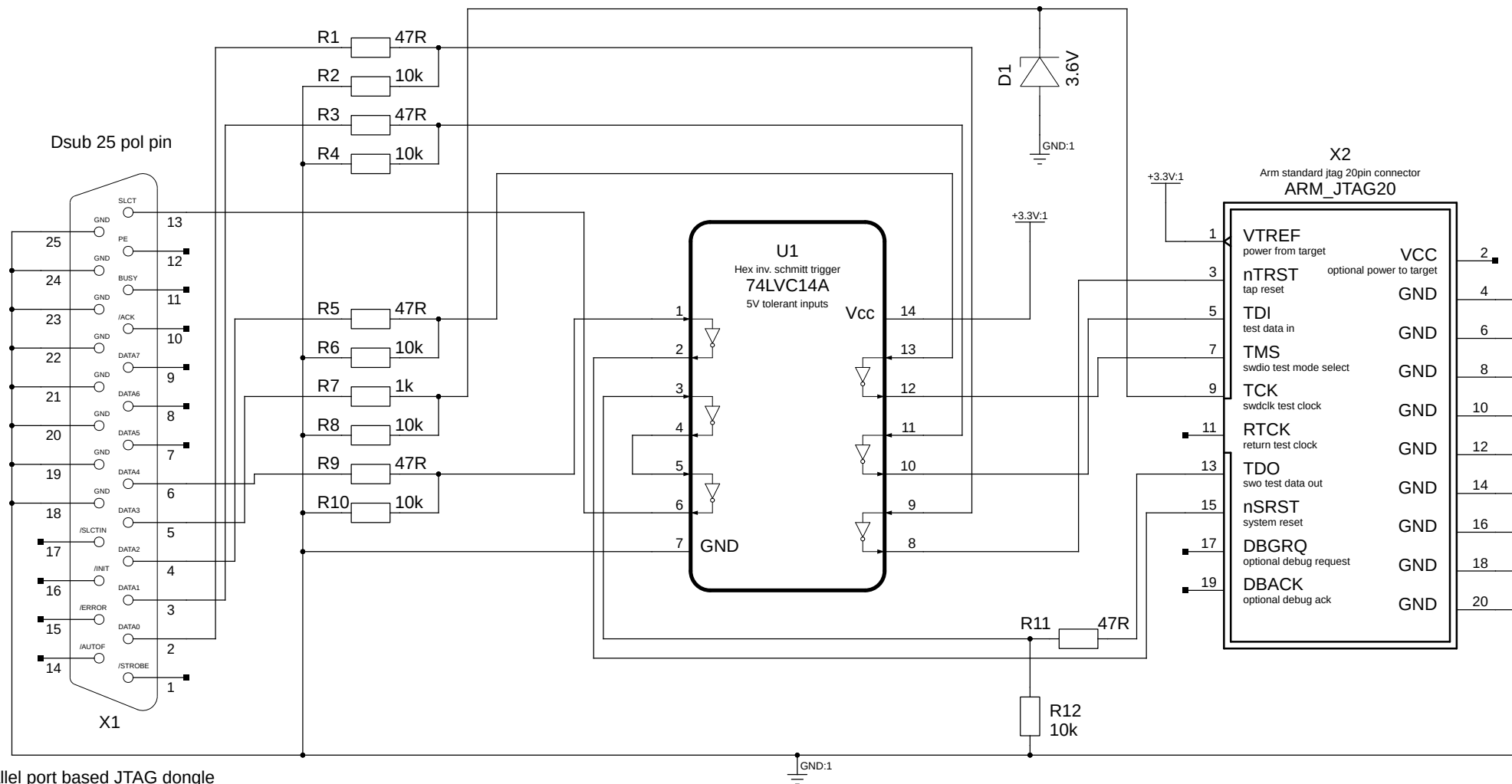




Design goal:

pp idle at all zeroes (or not connected) => jtag idle at all high except TCK low target at 3.3V

TDO -> select (status reg. 0x10, pin 13)

DATA0 (0x01 pin 2) -> nTRST

DATA1 (0x02 pin 3) -> TDI

DATA2 (0x04 pin 4) -> TMS

DATA3 (0x08 pin 5) -> TCK

DATA4 (0x10 pin 6) -> nSRST

All lines except TCK and TDO are inverted

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